ADC-XMC-STANDALONE
User Manual

Document Revision: 2.0
15/01/2024

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Table Of Contents

List of Tables

List of Figures

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1 Introduction

The ADC-XMC-STANDALONE is a standalone carrier for Alpha-Data XMCs. The board provides Ethernet, Serial COM, USB, SATA, M.2 PCIe, QSFP, FireFly, GPIO and DisplayPort IO options. To allow compatibility with various XMC board pinouts, a personality wiring card that matches the XMC pinout is used to route signals through to the IO interfaces.

Apart from the IO functionality, ADC-XMC-STANDALONE uses a single 15V-30V input power supply, and generates all supplies required by the XMC site internally. An on-board system monitor micro-controller provides voltage/current monitoring of the generated power supplies, as well as providing the capability to turn the supplies on/off via the micro USB interface. A USB to JTAG circuit is also provided, giving access to the JTAG chain without requiring an external JTAG box.

IO interface support is dependent on the XMC type fitted, as well as the configuration of that XMC board.

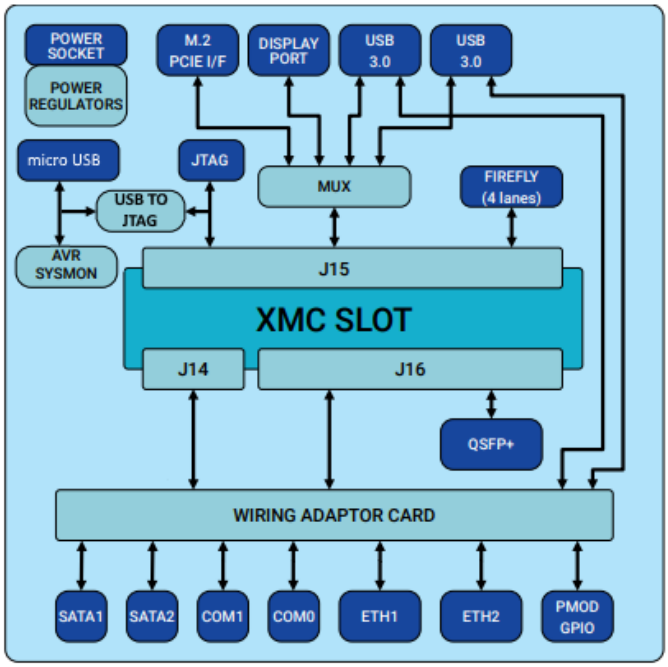

Figure 1 : ADC-XMC-STANDALONE Block Diagram

2 Board Features

The following photos highlight the various features of the ADC-XMC-STANDALONE

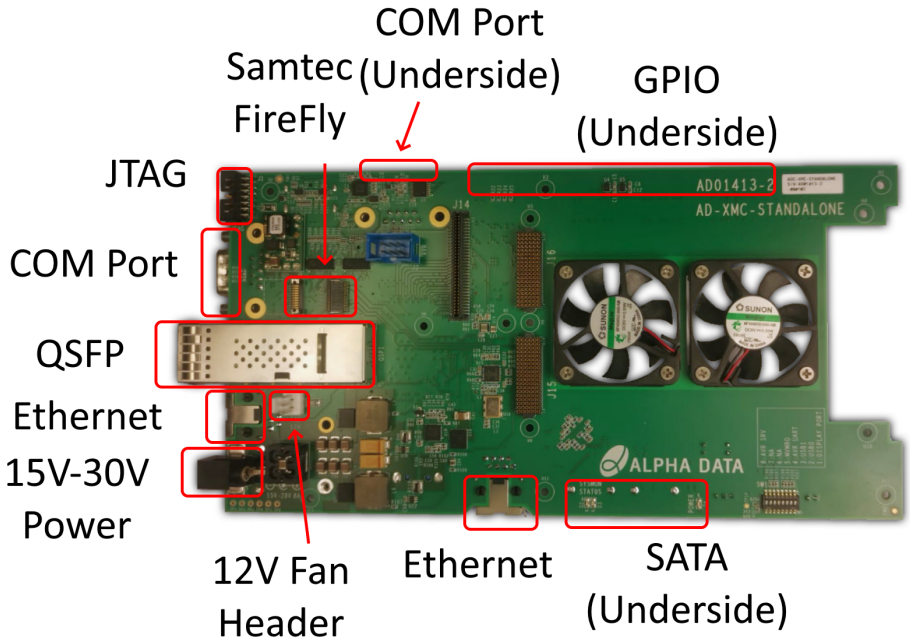

Figure 2 : ADC-XMC-STANDALONE Features

3 Switch Definitions

Default switch definitions are all OFF.

Switch	Description
SW1-1	DisplayPort Enable. Uses upper 2 PCIe lanes, limiting NVME devices to PCIe x2.
SW1-2	USB3 enable on USB-0 port J20. Uses PCIe lane 0, therefore effectively disabling NVME PCIe.
SW1-3	USB3 enable on USB-1 port J24. Uses PCIe lane 1, limiting NVME devices to PCIe x1.
SW1-4	Enables UART connection between system monitor and PMOD J3 pins 1, 2, 3 and J16 pins C15, F15, C14.
SW1-5	AVR service mode.
SW1-5	XMC MVMRO Enable.
SW1-6	Unused.
SW1-7	Unused.

Table 1 : Switch Definitions

4 M.2 Drive Selection

The ADC-XMC-STANDALONE has some components underneath the M.2 drive, so should only be used with single-sided M.2 NVMe drives.

5 Main Input Power Supply Requirements

The total power requirement for the main input supply will vary depending on the XMC board fitted, as well as the particular FPGA design within that board. A 60W supply would likely be more than enough for most FPGA designs before thermal limits of the device and heatsink become the limiting factor. Alpha-Data can provide a power supply estimator spreadsheet to estimate the total power requirements for a particular FPGA design with a particular XMC board.

Spec	Value
Voltage	15V-30V
Power	60W
Current	5A Max.
Connector	2.1mm x 5.5mm DC power plug, centre pin positive

Table 2 : Suggested Input Supply Specifications

6 Installation and Power Up

The required personality card should be attached to connectors J21, J22 and J23 on the read of the board prior to attaching the XMC card to J14, J15 and J16.

To power up the board, ensure that power switch SW2 is OFF, and connect a 15V-30V power supply. To turn the board ON, switch the power switch S2 to ON.

7 JTAG Interface

A USB to JTAG circuit is provided, giving access to the XMC JTAG interface without the need for an external programming box (e.g. Xilinx Platform Cable II). The USB to JTAG converter is compatibile with Vivado, and will appear in hardware manager as a Digilent device. A 14-pin JTAG header is also available, with an on-board multiplexer to switch between the 14-pin header or the USB to JTAG converter. The multiplexer selects the USB to JTAG circuit when a micro USB cable is attached.

8 GPIO Interface

The GPIO is provided as a set of connectors conforming to the Digilent PMOD specification: https://digilent.com/reference/_media/reference/pmod/pmod-interface-specification-1_2_0.pdf

The PMOD connectors are 12-pin connectors, with two 3.3V VCC pins, two GND pins and 8 data pins:

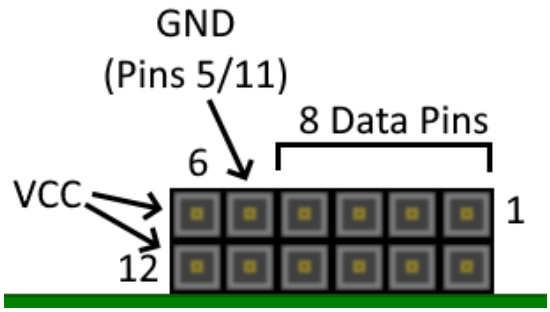

Figure 3 : PMOD Pinout

Maximum current draw on the VCC pins is not specified by the Digilent PMOD specification, but it recommends no more than approximately 100mA. On the ADC-XMC-STANDALONE, the 3.3V PMOD pins are connected directly to the main 3.3V power rail. This rail has a maximum current draw of 7A, although it is shared with the XMC board and other on-board devices, so total current draw of all PMOD devices should leave enough headroom for other devices on the 3.3V rail to operate.

There are a total of 5 PMOD connectors (J8, J3, J11, J12 and J13). The data pins of these connectors connect directly to the XMC J16 user defined IO pins. The GPIO pins connected to connector J8 also connect to the FireFly and QSFP sideband signals (I2C/RESET_L/INT_L/MODPRS_L), so are dual use. The FPGA pins that the PMOD data pins connect to are listed in section: Connector Pin Assignments when used with an XMC card. Some PMOD GPIO pins may be unconnected, depending on the number of GPIO pins available on the XMC card.

9 Current/Voltage Monitoring

The ADC-XMC-STANDALONE provides high-side current sense functionality on both the 12V and 3V3+3V3_AUX supplies. These values can be reported over the microUSB interface, using the alpha-data "avr2util" utility.

Avr2util for Windows and the associated USB driver can be downloaded here:
https://support.alpha-data.com/pub/firmware/utilities/windows/

Avr2util for Linux can be downloaded here:
https://support.alpha-data.com/pub/firmware/utilities/linux/

Use "avr2util.exe /?" to see all options.
For example "avr2util.exe /usbcom com4 display-sensors" will display all sensor values.

Note that 'com4' is used here as an example, and should be changed to match the com port number assigned under windows device manager

10 On-Board Generated Power Supplies

The ADC-XMC-STANDALONE generates the 3V3/3V3_AUX/12V0/-12V0 supplies required by the XMC site from a single 15V-30V input supply. Each supply has the following specifications:

Power supply	Voltage (V)	Max. current (A)	Monitoring
3V3_DIG	3.3	7.0 [1]	Voltage and current [1]
3V3_AUX	3.3 [2]	7.0 [1]	Voltage and current [1]
12V0_DIG	12.0	7.0	Voltage and current
-12V0_DIG	-12.0	1.5	Unmonitored

Table 3 : ADC-XMC-STANDALONE Power Supplies

[1] The 3V3_DIG and 3V3_AUX rails are generated from the same supply, so the maximum current is the combination of 3V3_AUX + 3V3_DIG. The current monitoring also measures the combined current.

[2] The 3V3_AUX rail is an always-on 3.3V auxiliary power supply from the 15V-30V input.

11 Connector Pin Assignments when used with an XMC card

The pinout depends on the personality board used. Select the correct table below for the pinout. Any pins not listed in the tables below are NC

11.1 ADM-XRC-9R1 pcb revision 3+ pinout

Unlisted PMOD pins are N/C when used with the ADM-XRC-9R1.

For ADC-XMC-STANDALONE rev2 PCBs, the PMOD connector silkscreen has pins 1-7 swapped with pins 8-12. The pinout in the table below is correct as per the PMOD spec, but does not match the silkscreen.

Dual use pins (e.g. GPIO4/PMOD_J8_10/FIREFLY_SDA) are also routed to the QSFP/FireFly module's sideband control signals, as well as the GPIO headers. The I2C signals (SDA/SCL) have 4k32 on-board pull-ups to 3.3V, and the RESET_L/MODPRS_L/INT_L signals have 12k0 pull-ups to 3.3V

Signal Name	J16 Pin	ADM-XRC-9R1 FPGA Pin	Function	Voltage Standard
QSFP_TX0_P	A1	B28	QSFP0 Tx+ (MGT128 3)	LVDS
QSFP_TX0_N	B1	B29	QSFP0 Tx- (MGT128 3)	LVDS
QSFP_RX0_P	A11	A31	QSFP0 Rx+ (MGT128 3)	LVDS
QSFP_RX0_N	B11	A32	QSFP0 Rx- (MGT128 3)	LVDS
QSFP_TX1_P	D1	C30	QSFP1 Tx+ (MGT128 2)	LVDS
QSFP_TX1_N	E1	C31	QSFP1 Tx- (MGT128 2)	LVDS
QSFP_RX1_P	D11	B33	QSFP1 Rx+ (MGT128 2)	LVDS
QSFP_RX1_N	E11	B34	QSFP1 Rx- (MGT128 2)	LVDS
QSFP_TX2_P	A3	D28	QSFP2 Tx+ (MGT128 1)	LVDS
QSFP_TX2_N	B3	D29	QSFP2 Tx- (MGT128 1)	LVDS
QSFP_RX2_P	A13	D33	QSFP2 Rx+ (MGT128 1)	LVDS
QSFP_RX2_N	B13	D34	QSFP2 Rx- (MGT128 1)	LVDS
QSFP_TX3_P	D3	E30	QSFP3 Tx+ (MGT128 0)	LVDS
QSFP_TX3_N	E3	E31	QSFP3 Tx- (MGT128 0)	LVDS
QSFP_RX3_P	D13	F33	QSFP3 Rx+ (MGT128 0)	LVDS
QSFP_RX3_N	E13	F34	QSFP3 Rx- (MGT128 0)	LVDS
SATA_TX0_P	A5	G30	SATA0 Tx+ (MGT129 3)	LVDS
SATA_TX0_N	B5	G31	SATA0 Tx- (MGT129 3)	LVDS
SATA_RX0_P	A15	H33	SATA0 Rx+ (MGT129 3)	LVDS
SATA_RX0_N	B15	H34	SATA0 Rx- (MGT129 3)	LVDS
SATA_TX1_P	D5	J30	SATA1 Tx+ (MGT129 2)	LVDS
SATA_TX1_N	E5	J31	SATA1 Tx- (MGT129 2)	LVDS
SATA_RX1_P	D15	K33	SATA1 Rx+ (MGT129 2)	LVDS

Table 4 : ADM-XRC-9R1 PCB revision 3+ pinout for J16 (continued on next page)

Signal Name	J16 Pin	ADM-XRC-9R1 FPGA Pin	Function	Voltage Standard
SATA_RX1_N	E15	K34	SATA1 Rx- (MGT129 2)	LVDS
GPIO_19	C7	D9	GPIO19/PMOD_J11_9	3.3V CMOS
GPIO_18	C8	C9	GPIO18/PMOD_J11_8	3.3V CMOS
GPIO_17	C9	B10	GPIO17/PMOD_J11_7	3.3V CMOS
GPIO_23	B19	F28	GPIO19/PMOD_J11_3	3.3V CMOS
GPIO_22	A19	F29	GPIO19/PMOD_J11_2	3.3V CMOS
GPIO_12	F14	C14	GPIO12/PMOD_J3_10	3.3V CMOS
GPIO_11	C14	C11	GPIO11/PMOD_J3_9	3.3V CMOS
GPIO_10	F15	K12	GPIO10/PMOD_J3_8	3.3V CMOS
GPIO_9	C15	E10	GPIO9/PMOD_J3_7	3.3V CMOS
GPIO_16	C10	B11	GPIO16/PMOD_J3_4	3.3V CMOS
GPIO_15	C11	A9	GPIO15/PMOD_J3_3	3.3V CMOS
GPIO_14	C12	E11	GPIO14/PMOD_J3_2	3.3V CMOS
GPIO_13	C13	D11	GPIO13/PMOD_J3_1	3.3V CMOS
GPIO_4	F18	A10	GPIO4/PMOD_J8_10/FIREFLY_SDA	3.3V CMOS
GPIO_3	C18	K10	GPIO3/PMOD_J8_9/QSFP_MODPRS_L	3.3V CMOS
GPIO_2	F19	C13	GPIO2/PMOD_J8_8/QSFP_SDA	3.3V CMOS
GPIO_1	C19	B13	GPIO1/PMOD_J8_7/QSFP_SCL	3.3V CMOS
GPIO_8	F16	E9	GPIO8/PMOD_J8_4/OPTICAL_INT_L	3.3V CMOS
GPIO_7	C16	H10	GPIO7/PMOD_J8_3/ OPTICAL_RESET_L	3.3V CMOS
GPIO_6	F17	C10	GPIO6/PMOD_J8_2/ FIREFLY_MODPRS_L	3.3V CMOS
GPIO_5	C17	H9	GPIO5/PMOD_J8_1/FIREFLY_SCL	3.3V CMOS

Table 4 : ADM-XRC-9R1 PCB revision 3+ pinout for J16

Signal Name	J14 Pin	Function	Voltage Standard
Front RJ1 pin1	1	Ethernet0 MD0+	1000-baseT
Front RJ1 pin2	3	Ethernet0 MD0-	1000-baseT
Front RJ1 pin3	7	Ethernet0 MD1+	1000-baseT
Front RJ1 pin4	2	Ethernet0 MD1-	1000-baseT
Front RJ1 pin5	4	Ethernet0 MD2+	1000-baseT
Front RJ1 pin6	9	Ethernet0 MD2-	1000-baseT
Front RJ1 pin7	8	Ethernet0 MD3+	1000-baseT
Front RJ1 pin8	10	Ethernet0 MD3-	1000-baseT
Side RJ1 pin1	13	Ethernet1 MD0+	1000-baseT
Side RJ1 pin2	15	Ethernet1 MD0-	1000-baseT
Side RJ1 pin3	19	Ethernet1 MD1+	1000-baseT
Side RJ1 pin4	14	Ethernet1 MD1-	1000-baseT
Side RJ1 pin5	16	Ethernet1 MD2+	1000-baseT
Side RJ1 pin6	21	Ethernet1 MD2-	1000-baseT
Side RJ1 pin7	20	Ethernet1 MD3+	1000-baseT
Side RJ1 pin8	22	Ethernet1 MD3-	1000-baseT
Front RJ2 pin3	43	COM1 Tx	RS232
Front RJ2 pin6	42	COM1 Rx	RS232
Side RJ2 pin3	47	COM2 Tx	RS232
Side RJ2 pin6	48	COM2 Rx	RS232
Front USB DP	27	USB Data+	USB
Front USB DM	25	USB Data-	USB
Front USB VBus	29	USB Vcc	5V0 Power
Side USB DP	28	USB Data+	USB
Side USB DM	26	USB Data-	USB
Side USB VBus	30	USB Vcc	5V0 Power

Table 5 : ADM-XRC-9R1 pcb revision 3+ pinout for J14

12 Dimensions

Dimension	Measurement
X PCB	219mm
X including connectors	230.15mm
Y PCB	112.5mm
Y including connectors	113.1mm

Table 6 : ADC-XMC-STANDALONE PCB dimensions

13 Order Code

ADC-XMC-STANDALONE/X/T

Name	Symbol	Configurations
XMC Personality Card	x	9R1 = ADM-XRC-9R1, 7Z1 = ADM-XRC-7Z1, 7Z2 = ADM-XRC-7Z2, 7Z4 = ADM-XRC-7Z4
XMC Connector Type	t	blank = XMC (VITA 42) Connectors, /X2 = XMC2 (VITA 61) Connectors

Table 7 : ADC-XMC-STANDALONE Order Code

Revision History

Date	Revision	Nature of Change
22 Feb 2021	1.0	Preliminary issue
18 May 2021	1.1	Added board diagram, added PMOD connector pin numbers, added 9R1 FPGA pin numbers
14 Oct 2021	1.2	Added description of the USB to JTAG, moved pin assignments to the end of the document
21 July 2022	1.4	Added P6 MGT refclk to 9R1 IO tables
05 October 2022	1.5	Added M.2 drive selection section
31 October 2022	1.6	Clarified PMOD due to pins 1-6 being swapped with 7-12
2 December 2022	1.7	Added switch defintions
4 January 2023	1.8	Added section describing GPIO PMOD connectors
15 November 2023	1.9	Fixing incorrect PMOD pin numbers in description for SW1-4
15 January 2024	2.0	Updating GPIO_22/GPIO_23 signal name to more accurately reflect the pin usage on the 9R1.

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